APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/343,872	06/30/1999	TUAN Q. DAO	5201-20400	8423

24319   7590   09/16/2003

LSI LOGIC CORPORATION
1621 BARBER LANE
MS: D-106 LEGAL
MILPITAS, CA 95035

EXAMINER
HUYNH, KIM T

ART UNIT	PAPER NUMBER
2189	

DATE MAILED: 09/16/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 07-01)

	Application No.	Applicant(s)
Office Action Summary	09/343,872	DAO ET AL.
	Examiner	Art Unit	
	Kim T. Huynh	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>30 June 2003</u> .

2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8 and 10-24* is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8 and 10-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

    If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All b)☐ Some * c)☐ None of:

        1.☐ Certified copies of the priority documents have been received.

        2.☐ Certified copies of the priority documents have been received in Application No. _____ .

        3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

    a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .

4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

1.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that

form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2.   Claim 15 is rejected under 35 U.S.C. 102(e) as being anticipated by Garnett et

al. (US Patent 6,141,718)

Garnett discloses a high-bandwidth bus which comprises:

- a plurality of local busses (fig.2, 22, 24, 26) each for transferring data

   between a processing device (fig.2, 14, 16) and an associated memory

   module (DMA, 133); (col.15, lines 7-24), (col.6, lines 45-65), i.e wherein

   bus 24 is connected to processing device 14 and 26 bus each connecting

   to processing device 16 and control by DMA and DMA is performing as

   memory access controlling between devices, it is inherent that DMA is

   part of memory module, col.1, line 52-col.2, line 37)

- a cross-bus (fig.6, 80) means for transferring data among the plurality of

   local bus means, wherein said cross-bus means is coupled to each of the

   plurality of local busses by a bridge (fig.1, 12) means; (col.6, lines 45-65),

   (col.10, lines 23-36)

- a memory controller means for setting said bridge means to provide

  processing devices with access to memory modules, wherein controller

  means is configured to provide highest priority for accesses from

  processing devices to the associated memory modules. (col.6, lines 45-

  67), (col.9, lines 36-51), (col.16, lines 32-67), (col.15, lines 7-24), wherein

  Routing matrix is mapping to different paths, the storage (memory) control

  access to bridge and bridge controller responsive to control signals, data

  and addresses on the paths to the devices and arbiter selecting priority

  first come first serve)

- wherein the local busses each include two unidirectional (fig.6, 92, 94, 96)

  bit lines for each data bit and at least the cross-bus includes two

  unidirectional bit lines for each data bit, (wherein, multiplexer, (fig.9, 143),

  logically mapping for routing for each outgoing bit line that selects (col.6,

  lines 45-65), (col.10, lines 23-36), (fig.6, 94, 96, 92, the paths of data lines

  , wherein data routing via these paths from source to devices enhance

  unidirectional bit lines)

3.   Claims 16-24 is rejected under 35 U.S.C. 102(e) as being anticipated by

Funaya et al. (US 6,263,393)

       As per claim 16, Funaya discloses a high-bandwidth bus system which

comprises:

- a plurality of local memory busses each for transferring data between a processing device and an associated memory module; (col.6, lines 35-48)

- one or more local intersect busses for transferring data between the plurality of local memory busses, wherein said local intersect busses are coupled to each of the plurality of local memory busses by four multiplexers at each intersection; and (col.4, line 61-col.5, line 22)

- a memory controller means for setting each multiplexer to provide processing devices with access to memory modules, wherein the memory controller means is configured to provide highest priority for accesses from processing devices to the associated memory modules (col.4, line 47-col.5, line 48)

- wherein the local memory busses each include two unidirectional bit lines for each data bit and the local intersect busses includes two unidirectional bit lines for each data bit. (col.4, line 47-col.5, line 48), (col.6, line 3-67)

As per claim 17, Funaya discloses wherein the four multiplexers forward data between a processing device and a memory device with essentially no latency delay. (col.4, line 47-50)

As per claim 18, Funaya discloses the bus system further comprising a memory management unit that includes a DMA controller coupled to the local intersect

busses and configurable to transfer a block of data between said memory

modules. (col.4, line 47-col.5, line 48)

As per claim 19, Funaya discloses wherein the memory management unit

includes an interrupt controller configurable to assert an interrupt signal to said

processing devices after completing a block transfer of data. (col.6, lines 3-67)

As per claim 20, Funaya discloses wherein the memory management unit

includes one or more request queues, wherein said one or more request queues

includes a single transfer queue configured to store access requests relating to

single data word transfers. (col.5, line 35-67), (col.6, lines 35-67)

As per claim 21, Funaya discloses wherein said one or more request queues

includes a block transfer queue configured to store access requests relating to

block data transfers. (col.6, lines 35-67)

As per claim 22, Funaya discloses wherein said one or more request queues

includes a message transfer queue configured to store message transfer

requests. (col.6, lines 35-67)

As per claim 23, Funaya discloses wherein the memory management unit

includes an interrupt controller configurable to assert an interrupt signal to a

processing device that is an addressee of a message transfer request. (col.6,

lines 35-48)

As per claim 24, Funaya discloses the bus system further comprising port logic

connected to the plurality of local memory busses and configured to couple to the

processing devices, wherein the port logic is further coupled to the memory

management unit and configured to prevent writes to protected memory. (col.6,

lines 35-67)

Claim Rejections - 35 USC § 103

4.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set
> forth in section 102 of this title, if the differences between the subject matter sought to be patented and
> the prior art are such that the subject matter as a whole would have been obvious at the time the
> invention was made to a person having ordinary skill in the art to which said subject matter pertains.
> Patentability shall not be negatived by the manner in which the invention was made.

5.   Claims 1-8, 10-14 are rejected under 35 U.S.C. 103(a) as being unpatentable

over Garnett et al. (US Patent 6,141,718) in view of Funaya et al. (US Patent 6,263,393)

As per claim 1, Garnett discloses a data transfer apparatus that comprises:

- a plurality of busses (fig.1, ie. 24, 26, D-bus) each configured to couple a

  processing device (fig.1, ie. 14, 16) to a corresponding memory

  module;(col.1, lines 52-65), (col.5, lines 18-54)

- at least one cross-bus (fig.6, 80) coupled to each of the plurality of busses

  by one or more bus bridges, wherein the bus bridge (fig.14, 12) each

  include a multiplexer (fig.9, 143) that are configurable to steer signals

  from the bus to the cross-bus, and are further configurable to steer signals

  from the cross-bus to the bus; (col.6, lines 45-65), (col.10, lines 23-36)

- a memory management unit configured to receive memory access

  requests from a plurality of processing devices and to responsively

  configured the bus bridges to steer address and data signals accordingly.

  (col.9, lines 36-51),

- wherein the plurality of busses includes two unidirectional (fig.6, 92, 94,

  96) bit lines for each data bit and at least one cross-bus includes two

  unidirectional bit lines for each data bit, and wherein the bus bridges

  include a multiplexer (fig.9, 143) for each outgoing bit line that selects from

  three other incoming bit lines. (col.6, lines 45-65), (col.10, lines 23-36),

  (fig.6, 94, 96, 92), paths of data lines , wherein data routing via these

  paths from source to devices enhance unidirectional bit lines)

  Garnett discloses all the limitations as above except a set of

multiplexers However, Funaya's system has multiple of multiplexers.

Funaya's system includes busses system control by a switch module which

includes multiple of bus bridges each bridge include multiplexer which mux all

busses and each bus correspond to each device. (col.5, lines 6-22)

  It would have been obvious to one having ordinary skills in the art at

the time the invention was made to incorporate Funaya's teaching into

Garnett's method   so as to have the availability of the switch is to lowered

and the throughput of the bus switch is necessitated to be decreased. (col.3,

lines 60-63)

As per claim 11, Garnett discloses a method for transferring data between a set

of memory modules and a set of processor units, wherein the method comprises:

- said processing units (fig.2, 14, 16) providing transfer requests to a

  memory manager; (col.15, lines 7-36), wherein processor set address

from which to read and transfer, DMA emulates a device bus sending

identical DMA requests)

- said memory manager setting a router(fig.6, 80) in a conflict-free

  access pattern in response to said transfer requests, wherein setting

  said router includes: (col.16, lines 32-40)

- said memory manager providing control signals to bus bridges that

  couple local busses between a memory module and a processing

  device to a cross-bus between the local busses; and ;(col.1, lines 52-

  65), (col.5, lines 18-54),

- wherein the plurality of busses includes two unidirectional (fig.6, 92,

  94, 96) bit lines for each data bit and at least one cross-bus includes

  two unidirectional bit lines for each data bit, and wherein the bus

  bridges include a multiplexer (fig.9, 143) for each outgoing bit line that

  selects from three other incoming bit lines. (col.6, lines 45-65), (col.10,

  lines 23-36), (fig.6, 94, 96, 92), paths of data lines , wherein data

  routing via these paths from source to devices enhance unidirectional

  bit lines)

- said processing units accessing memory modules via said router.

  ;(col.1, lines 52-65), (col.5, lines 18-54)

As per claims 2, 13, Garnett discloses the memory management unit includes a

DMA controller coupled to the cross-bus and configurable to transfer a data

between said memory modules. (col.9, lines 32-51), (col.6, lines 9-15); however

Garnett fails to disclose controller configurable to transfer a block of data.

Garnett fails to disclose controller configurable for transferring a block

data. However, Funaya discloses the word type identification bits are used by the

switch module for discriminating between a header of a transaction cell, data of a

transaction cell, a delimiter of a transaction cell and an invalid word. Switch

transfers the distributed word to one of the output ports of the switch module

according to the destination port number of a cell in which the word is included

(col.5, lines 35-48)

It would have been obvious to one having ordinary skills in the art at

the time the invention was made to incorporate Funaya's teaching into

Garnett's method   so as to have the availability of the switch is to lowered

and the throughput of the bus switch is necessitated to be decreased. (col.3,

lines 60-63)

As per claim 3, Garnett discloses the memory management unit includes an

interrupt controller (fig.8, 134) configurable to assert an interrupt signal to said

processing devices after completing transfer data. (col.16, lines 32-67), (col.17,

lines 1-26) wherein busy condition implies not allowing data transfer until

complete)

As per claims 4,5, 6, 14, Garnett discloses the memory management unit

includes one or more request queues, wherein said one or more request queues

includes a single transfer queue configured to store access requests relating to

data transfers. (col.10, lines 23-61), wherein signals are held in buffer (fig.9, 149)

implies queue, ready to be selected for transferring)

However Garnett fails to disclose single word of data, block data or

message transfer.

Garnett fails to disclose controller configurable for transferring a single

data word, block data, message transfer. However, Funaya discloses the word

type identification bits are used by the switch module for discriminating between

a header of a transaction cell, data of a transaction cell, a delimiter of a

transaction cell and an invalid word. Switch transfers the distributed word to one

of the output ports of the switch module according to the destination port number

of a cell in which the word is included (col.5, lines 35-48)

It would have been obvious to one having ordinary skills in the art at

the time the invention was made to incorporate Funaya's teaching into

Garnett's method   so as to have the availability of the switch is to lowered

and the throughput of the bus switch is necessitated to be decreased. (col.3,

lines 60-63)

As per claim 7, Garnett discloses the memory management unit includes an

interrupt controller (fig.8, 134) configurable to assert an interrupt signal to a

processing device that is an addressee of a data transfer request. (col.9, lines

36-55)

As per claim 8, Garnett discloses data transfer apparatus further comprising port

logic (fig.6, 88) connected to the plurality of busses and configured to couple to

the processing devices, wherein the port logic is further coupled to the memory

management unit and configured to prevent writes to-protected memory. (col.2,

lines 19-29) , (col.13, lines 10-13)

As per claim 10, plurality of busses includes at least three busses. (fig.6, 22, 24,

26), (col.4, lines 21-25)

As per claim 12, Garnett discloses wherein before setting said router(fig.6, 80),

said memory manager determines said conflict-free access pattern in

accordance with assigned priorities for each transfer request. (col.16, lines 32-

67, setting priority first come first serve implies conflict-free)

Response to Amendment

6.   Applicant's amendment filed on 6/30/03 have been fully considered but are moot

in view of the new ground(s) of rejection.

        a. In response to applicant's argument that memory module cited by examiner is

not associated with a particular processing device and i/o busses are not local busses

between a processing device and associated module. As Garnett notes at (col.1, lines

52-col.2, line 37) wherein bus 24 is connected to processing device 14 and 26 bus

each connecting to processing device 16 and controller by DMA and DMA is performing

as memory access controlling between devices, it is inherent that DMA is part of

memory module.

        b. In response to applicant's argument that Garnett does not teach a set of

multiplexers and requested the examiner to support. Funaya's system has multiple of

multiplexers. Funaya's system includes busses system control by a switch module

which includes multiple of bus bridges each bridge include multiplexer which mux all

busses and each bus correspond to each device. (col.5, lines 6-22)

Conclusion

8.   *Any inquiry concerning this communication or earlier communications from the examiner should*

be directed to Kim Huynh whose telephone number is (703)305-5384 or via e-mail addressed to

[kim.huynh3@uspto.gov]. The examiner can normally be reached on M-F 8:30AM- 6:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark

Rinehart can be reached on (703) 305-4815 or via e-mail addressed to [mark.rinehart@uspto.gov]. The

fax phone numbers for the organization where this application or proceeding is assigned are (703)872-

9306 for regular communications and After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be

directed to the receptionist whose telephone number is (703)306-5631.

Kim Huynh

Sept. 7, 2003

MARK H. RINEHART
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100